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Terms	Documents
L1 and ((hot or live) adj1 (plug$4 or connection or insert$3))	28

Database:
US Pre-Grant Publication Full-Text Database
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Search: L4

Refine Search

Recall Text | Clear | Interrupt

Search History

DATE: Tuesday, July 20, 2004 Printable Copy Create Case

Set Name side by side	Query	Hit Count	Set Name result set
DB=USPT,USOC; PLUR=YES; OP=OR			
L4	L1 and ((hot or live) adj1 (plug$4 or connection or insert$3))	28	L4
L3	L1 same ((hot or live) adj1 (plug$4 or connection or insert$3))	0	L3
L2	L1 same((hot or live) adj1 (plug$4 or connection or insert$3))	0	L2
L1	switch near10 power near10 ground	5806	L1

END OF SEARCH HISTORY

h e b b cg b e e ch

Refine Search

Search Results -

Terms	Documents
L4	0

Database:
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DB=USPT,USOC; PLUR=YES; OP=OR			
L4	L1 and ((hot or live) adj1 (plug$4 or connection or insert$3))	28	L4
L3	L1 same ((hot or live) adj1 (plug$4 or connection or insert$3))	0	L3
L2	L1 same((hot or live) adj1 (plug$4 or connection or insert$3))	0	L2
L1	switch near10 power near10 ground	5806	L1

END OF SEARCH HISTORY

h e b b cg b e e ch

Refine Search

Search Results -

Terms	Documents
L1 and (ground same power same switch same disabl$3)	6

Database:
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IBM Technical Disclosure Bulletins

Search: L3

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L3	L1 and (ground same power same switch same disabl$3)	6	L3
L2	L1 and (ground same power same switch)	53	L2
L1	710/301-304.ccls.	822	L1

END OF SEARCH HISTORY

Refine Search

Search Results -

Terms	Documents
L3	0

Database:
US Pre-Grant Publication Full-Text Database
US Patents Full-Text Database
US OCR Full-Text Database
EPO Abstracts Database
JPO Abstracts Database
Derwent World Patents Index
IBM Technical Disclosure Bulletins

Search: L4

Refine Search

Recall Text Clear Interrupt

Search History

DATE: Tuesday, July 20, 2004 Printable Copy Create Case

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DB=USPT,USOC; PLUR=YES; OP=OR			
L3	L1 and (ground same power same switch same disabl$3)	6	L3
L2	L1 and (ground same power same switch)	53	L2
L1	710/301-304.ccls.	822	L1

END OF SEARCH HISTORY

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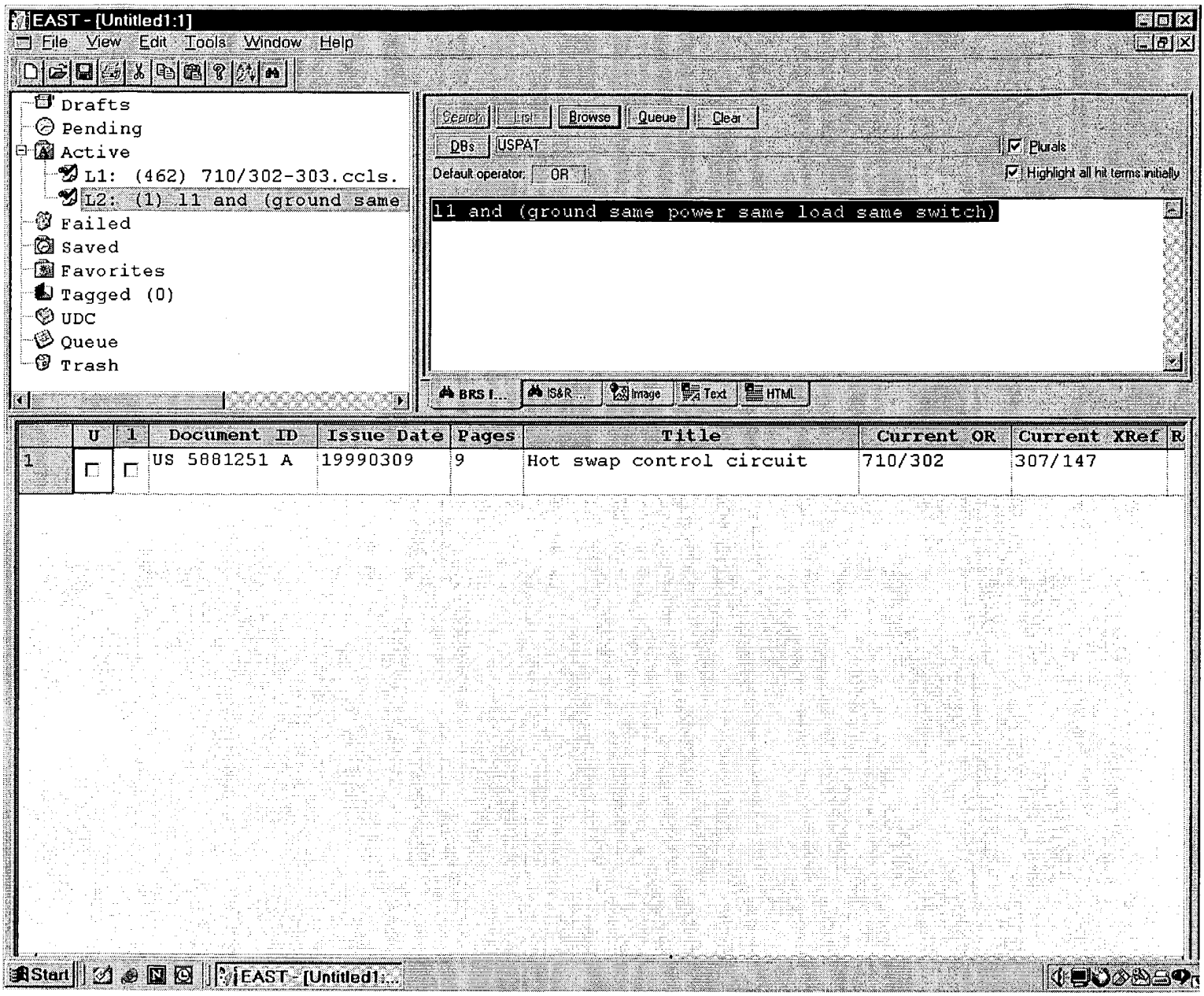
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File View Edit Tools Window Help
Drafts
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L1: (462) 710/302-303.ccls.
L2: (1) l1 and (ground same
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l1 and (ground same power same load same switch)
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1
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Title
Current OR
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1
US 5881251 A
19990309
9
Hot swap control circuit
710/302
307/147
Start
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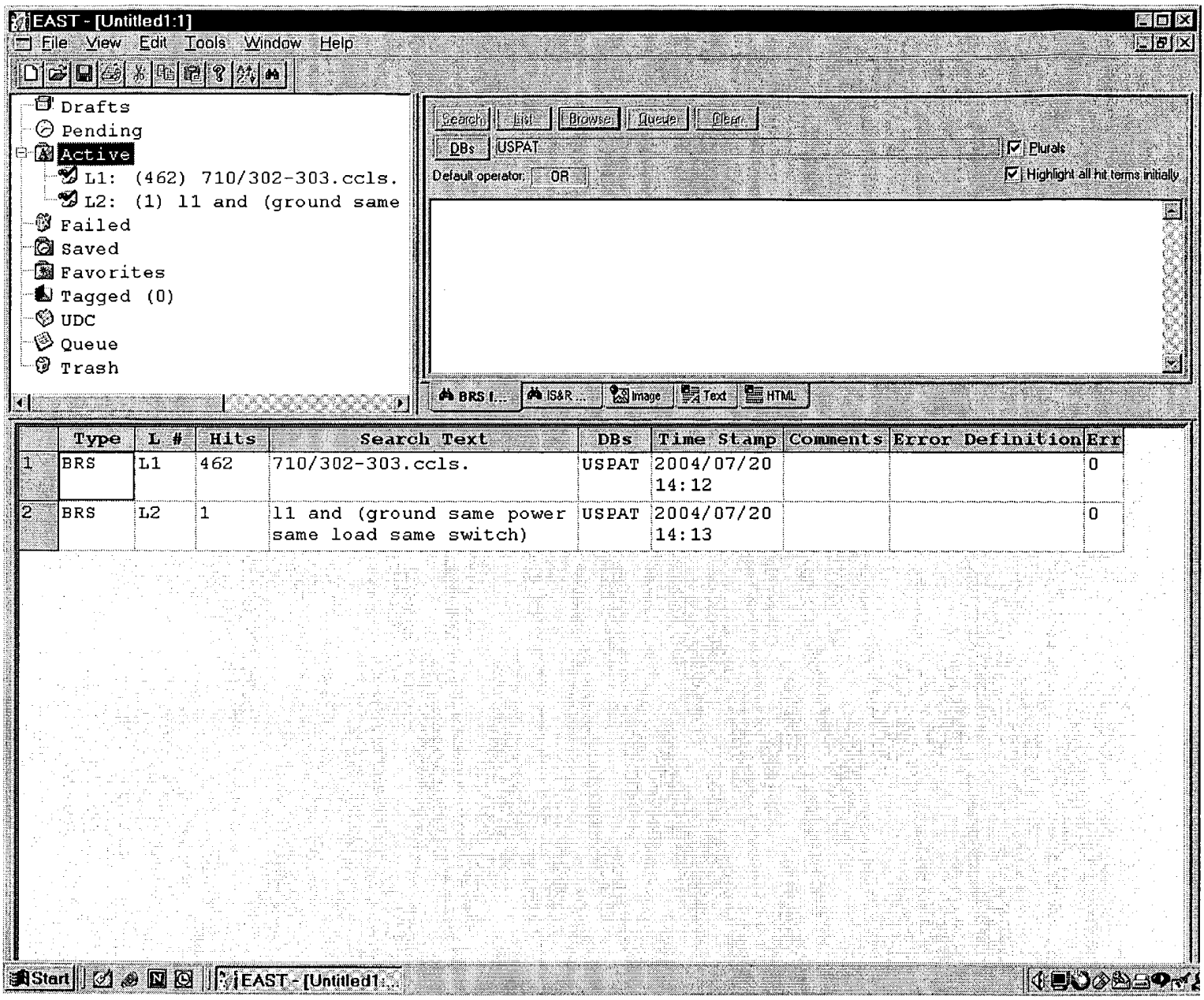

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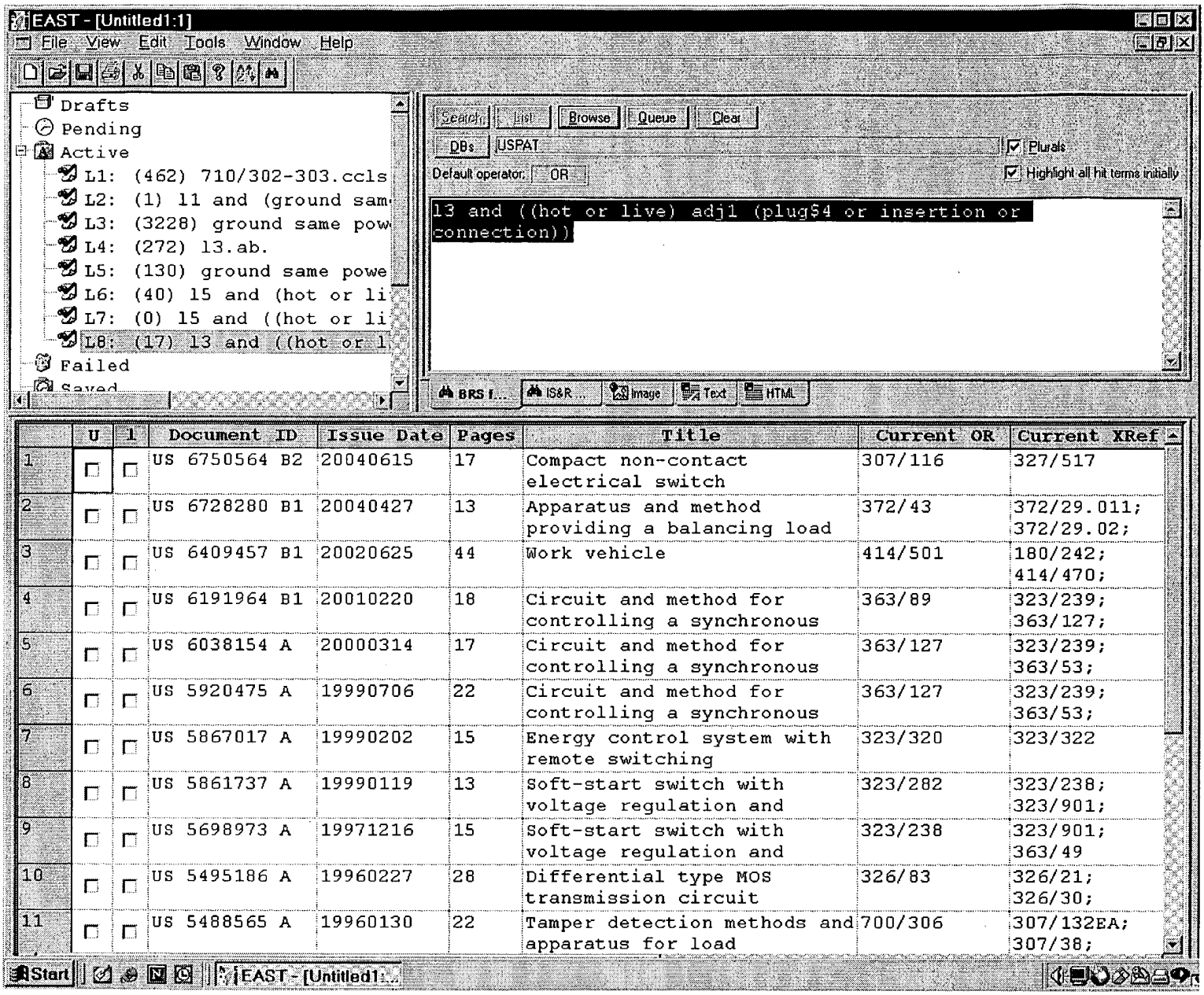
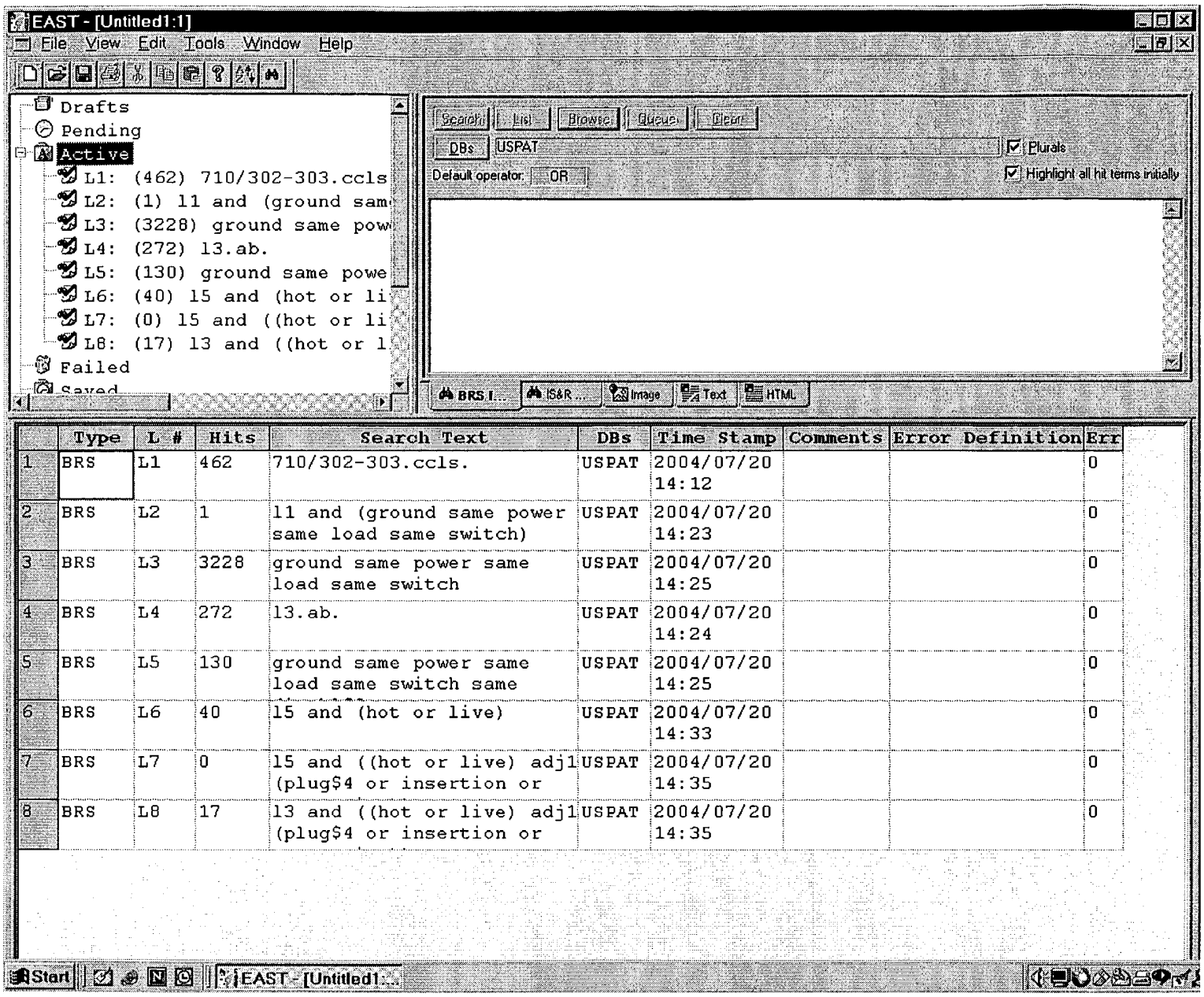
2	BRS	L2	1	l1 and (ground same power same load same switch)	USPAT	2004/07/20 14:13			0



	U	1	Document ID	Issue Date	Pages	Title	Current OR	Current XRef
1	☐	☐	US 6750564 B2	20040615	17	Compact non-contact electrical switch	307/116	327/517
2	☐	☐	US 6728280 B1	20040427	13	Apparatus and method providing a balancing load	372/43	372/29.011; 372/29.02;
3	☐	☐	US 6409457 B1	20020625	44	Work vehicle	414/501	180/242; 414/470;
4	☐	☐	US 6191964 B1	20010220	18	Circuit and method for controlling a synchronous	363/89	323/239; 363/127;
5	☐	☐	US 6038154 A	20000314	17	Circuit and method for controlling a synchronous	363/127	323/239; 363/53;
6	☐	☐	US 5920475 A	19990706	22	Circuit and method for controlling a synchronous	363/127	323/239; 363/53;
7	☐	☐	US 5867017 A	19990202	15	Energy control system with remote switching	323/320	323/322
8	☐	☐	US 5861737 A	19990119	13	Soft-start switch with voltage regulation and	323/282	323/238; 323/901;
9	☐	☐	US 5698973 A	19971216	15	Soft-start switch with voltage regulation and	323/238	323/901; 363/49
10	☐	☐	US 5495186 A	19960227	28	Differential type MOS transmission circuit	326/83	326/21; 326/30;
11	☐	☐	US 5488565 A	19960130	22	Tamper detection methods and apparatus for load	700/306	307/132EA; 307/38;



	Type	L #	Hits	Search Text	DBs	Time Stamp	Comments	Error Definition	Err
1	BRS	L1	462	710/302-303.ccls.	USPAT	2004/07/20 14:12			0
2	BRS	L2	1	l1 and (ground same power same load same switch)	USPAT	2004/07/20 14:23			0
3	BRS	L3	3228	ground same power same load same switch	USPAT	2004/07/20 14:25			0
4	BRS	L4	272	l3.ab.	USPAT	2004/07/20 14:24			0
5	BRS	L5	130	ground same power same load same switch same	USPAT	2004/07/20 14:25			0
6	BRS	L6	40	l5 and (hot or live)	USPAT	2004/07/20 14:33			0
7	BRS	L7	0	l5 and ((hot or live) adj1 (plug$4 or insertion or	USPAT	2004/07/20 14:35			0
8	BRS	L8	17	l3 and ((hot or live) adj1 (plug$4 or insertion or	USPAT	2004/07/20 14:35			0

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power and ground and switch and (hot or live) Search

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Results Key:
JNL = Journal or Magazine **CNF** = Conference **STD** = Standard

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1 **A ladder thermoelectric parallelepiped generator**
Ottarsson, G.K.;
Thermoelectrics, 2003 Twenty-Second International Conference on - ICT , 17 Aug. 2003
Pages:585 - 588

[Abstract] [PDF Full-Text (1390 KB)] **IEEE CNF**

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2 **Safety procedures for working on de-energized EHV lines sharing common right of way**
Dwivedi, P.K.; Saxena, N.S.; Kumar, P.; Jain, N.K.; Baba, K.V.S.;
Power Delivery, IEEE Transactions on , Volume: 7 , Issue: 3 , July 1992
Pages:1371 - 1378

[Abstract] [PDF Full-Text (588 KB)] **IEEE JNL**

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3 **Effect of floating conducting objects on critical switching impulse breakdown of air insulation**
Rizk, F.A.M.;
Power Delivery, IEEE Transactions on , Volume: 10 , Issue: 3 , July 1995
Pages:1360 - 1370

[Abstract] [PDF Full-Text (804 KB)] **IEEE JNL**

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4 **IEEE standard for gas-insulated, metal-enclosed disconnecting, interrupter, and grounding switches**

ANSI/IEEE Std C37.38-1989 , 2 Oct. 1989
[Abstract] [PDF Full-Text (92 KB)] **IEEE STD**

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5 **A Pre-TR Tube for High Mean Power Duplexing**
Lomer, P.D.; Downton, D.W.;
Microwave Theory and Techniques, IEEE Transactions on , Volume: 8 , Issue: 6 , Nov 1960
Pages:654 - 659

[Abstract] [PDF Full-Text (968 KB)] IEEE JNL

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6 **Fast modeling of core switching noise on distributed LRC power gri ULSI circuits**
Li-Rong Zheng; Tenhunen, H.;
Advanced Packaging, IEEE Transactions on [see also Components, Packaging Manufacturing Technology, Part B: Advanced Packaging, IEEE Transactions on] , Volume: 24 , Issue: 3 , Aug. 2001
Pages:245 - 254

[Abstract] [PDF Full-Text (272 KB)] IEEE JNL

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7 **Advanced semiconductor switches for EM launchers**
Singh, H.; Hummer, C.R.;
Magnetics, IEEE Transactions on , Volume: 37 , Issue: 1 , Jan. 2001
Pages:394 - 397

[Abstract] [PDF Full-Text (76 KB)] IEEE JNL

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8 **Transition density: a new measure of activity in digital circuits**
Najm, F.N.;
Computer-Aided Design of Integrated Circuits and Systems, IEEE Transaction on , Volume: 12 , Issue: 2 , Feb. 1993
Pages:310 - 323

[Abstract] [PDF Full-Text (1068 KB)] IEEE JNL

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9 **Separable connector switching performance**
Filter, R.; Jones, A.S.;
Power Delivery, IEEE Transactions on , Volume: 5 , Issue: 1 , Jan. 1990
Pages:435 - 441

[Abstract] [PDF Full-Text (588 KB)] IEEE JNL

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10 **True low-voltage flash memory operations**
Min-Hwa Chi; Bergemont, A.;
Nonvolatile Memory Technology Conference, 1996., Sixth Biennial IEEE International , 24-26 June 1996
Pages:94 - 98

[Abstract] [PDF Full-Text (484 KB)] IEEE CNF

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11 **Status of the pulsed power system for the PHELIX kilojoule/petaw laser at GSI Darmstadt**
Tauschwitz, A.; Dewald, E.; Becker de-Mos, B.; Samek, S.; Reinhard, I.; Kuh
Power Modulator Symposium, 2002 and 2002 High-Voltage Workshop. Confer Record of the Twenty-Fifth International , 30 June-3 July 2002

Pages:532 - 535

[Abstract] [PDF Full-Text (358 KB)] **IEEE CNF**

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12 **Pulsed power system for the PHELIX kilojoule/petawatt-laser at G Darmstadt**
Tauschwitz, A.; Dewald, E.; De-Mos, B.B.; Reinhard, I.; Roth, M.; Borneis, S. Kuhl, T.;
Pulsed Power Plasma Science, 2001. PPPS-2001. Digest of Technical Papers , Volume: 2 , 17-22 June 2001
Pages:1536 - 1538 vol.2

[Abstract] [PDF Full-Text (296 KB)] **IEEE CNF**

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13 **Pulsed power system for the PHELIX kilojoule/petawatt-laser at G Darmstadt**
Tauschwitz, A.; Dewald, E.; Mos, B.B.D.; Reinhard, I.; Borneis, S.; Kuhl, T.; M.;
Pulsed Power Plasma Science, 2001. IEEE Conference Record - Abstracts , 17 June 2001
Pages:442

[Abstract] [PDF Full-Text (50 KB)] **IEEE CNF**

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14 **Basic concepts and auto-check for clearing procedures**
Parise, G.; Hesla, E.;
Industrial and Commercial Power Systems Technical Conference, 1999 IEEE. May 1999
Pages:10 pp.

[Abstract] [PDF Full-Text (468 KB)] **IEEE CNF**

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Separable connector switching performance

Filter, R. Jones, A.S.
Ontario Hydro, Toronto, Ont., Canada ;

This paper appears in: **Power Delivery, IEEE Transactions on**

Publication Date: Jan. 1990
On page(s): 435 - 441
Volume: 5 , Issue: 1
ISSN: 0885-8977
Reference Cited: 10
CODEN: ITPDE5
Inspec Accession Number: 3631930

Abstract:
Laboratory loadbreak testing of 25 kV class separable insulated connectors su **switching** reliability achieved in the field will vary between 93.5% and 99.9% on the type of tool used, the condition of the connector system, the circuit vo loading, and **ground** plane proximity. A survey of user reliability requirement that a reliability of at least 99.7% is needed to retain separable connector **sw** a viable means of providing URD flexibility. It is concluded that in order to ma required reliability for **live switching**, the best operating tools and the best s connector system components must be used

Index Terms:
electric connectors reliability **switching** testing 25 kV URD flexibility circuit volta plane proximity insulated connectors loadbreak testing separable connector **switchi** **switching** reliability

Documents that cite this document
There are no citing documents available in IEEE Xplore at this time.

Search Results [PDF FULL-TEXT 588 KB] PREV NEXT DOWNLOAD CITATION

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L4: Entry 2 of 28 File: USPT Apr 6, 2004

DOCUMENT-IDENTIFIER: US 6718472 B1
TITLE: System for suspending power to a field replaceable unit upon receiving fault signal and automatically reapplying power thereto after the replacement unit is secured in position

Detailed Description Text (6):
Some of the devices, including an Ethernet (E-NET) interface 28 and a Small Computer System Interface (SCSI) interface 29, are permanently connected to the device bus 22, but other I/O devices such as I/O devices 30, 31 and 32 can be hot insertable into individual switched slots 33, 34 and 35. Dynamic field effect transistor (FET) switching can be provided for the slots 33, 34 and 35 to enable hot insert ability of the devices such as devices 30, 31 and 32. The provision of the FETs enables an increase in the length of the D bus 22 as only those devices which are active are switched on, reducing the effective total bus length. It will be appreciated that the number of I/O devices which may be connected to the D bus 22, and the number of slots provided for them, can be adjusted according to a particular implementation in accordance with specific design requirements.

Detailed Description Text (53):
FIG. 12 is a circuit diagram of main power control logic 650. This shows a power switch 682 in the form of a semiconductor device (here an N-channel field effect transistor), and a switch control circuit 670 for controlling the power switch 682. The switch control circuit 670 includes an input 672 connected to the debounced interlock signal line 664, a power input 680 connected to the main power line 660, a gate output 678 connected to a gate of the switch 682, a ground connection 676 connected to ground and a sense input 674 connected to a power overload sensing circuit 684. The switch control circuit 670 also includes enable, shut down and status connections that are not relevant to an understanding of the present invention.

Detailed Description Text (66):
Subsequently, in Step S20, a maintenance engineer will remove the PCI carrier assembly 216 from the chassis 200. This will involve opening the injector lever 542, which in turn opens the microswitch 540. This results in the interlock signal line 536 no longer being tied to ground, whereby the removal of the interlock signal can be detected by the switch control circuit 670 of the main power control logic 650 via the debounce logic 652. The standby power control logic 652 is also responsive to removal of the interlock signal on opening the microswitch 540 to cut the supply of standby power on line 626/526 to the non-volatile memory 230.

L4: Entry 2 of 28 File: USPT Apr 6, 2004

US-PAT-NO: 6718472
DOCUMENT-IDENTIFIER: US 6718472 B1

TITLE: System for suspending power to a field replaceable unit upon receiving fault signal and automatically reapplying power thereto after the replacement unit is secured in position

DATE-ISSUED: April 6, 2004

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Garnett; Paul J.	Camberley			GB

ASSIGNEE-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY	TYPE CODE
Sun Microsystems, Inc.	Santa Clara	CA			02

APPL-NO: 09/ 416001 [PALM]
DATE FILED: October 8, 1999

INT-CL: [07] G06 F 1/28

US-CL-ISSUED: 713/300; 713/330, 713/340, 710/10, 710/15, 710/103
US-CL-CURRENT: 713/300; 710/10, 710/15, 710/302, 713/330, 713/340

FIELD-OF-SEARCH: 710/103, 710/10, 710/15, 347/19, 347/23, 347/36, 713/102, 713/330, 713/340, 713/300

PRIOR-ART-DISCLOSED:

U.S. PATENT DOCUMENTS

Search Selected Search ALL Clear

	PAT-NO	ISSUE-DATE	PATENTEE-NAME	US-CL
☐	6105090	August 2000	Fosmo	710/103
☐	6192434	February 2001	Wallach et al.	710/103
☐	6227642	May 2001	Hanabusa et al.	347/19
☐	6363493	March 2002	Williams	714/1

ART-UNIT: 2154

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PRIMARY-EXAMINER: Lee; Thomas

ASSISTANT-EXAMINER: Hu; Jinsong

ATTY-AGENT-FIRM: Meyertons Hood Kivlin Kowert & Goetzel, P.C. Kivlin; B. Noel

ABSTRACT:

A power sub-system controls a supply of power to a field replaceable unit for electronic equipment. The power sub-system includes a power controller that is arranged, in response to the detection of a fault, to switch off the supply of power to a field replaceable unit. The power controller is then responsive to a sequence of two events to switch on the supply of power to the field replaceable unit. The first event is a first change in state of an interlock signal indicative of the field replaceable unit being released. The second event is a change of state of the interlock signal indicative of a field replaceable unit being secured in position. Automatic power management can thus provided with requiring a maintenance engineer to restore power manually, this being achievable simply by the removal and replacement of the field replaceable unit. The field replaceable unit includes an interlock mechanism for locking the field replaceable unit in the electronic equipment. An interlock switch is operated by the interlock mechanism and causes an interlock signal line to be connected to a source of the predetermined potential when the interlock mechanism locks the field replaceable unit in the electronic equipment. It is changes on the interlock signal line that are detected by the power controller.

32 Claims, 16 Drawing figures

Previous Doc Next Doc Go to Doc#

First Hit Fwd Refs Previous Doc Next Doc Go to Doc#
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L4: Entry 13 of 28 File: USPT Jul 27, 1999

DOCUMENT-IDENTIFIER: US 5930110 A
TITLE: Computer system having detachable expansion unit

Detailed Description Text (90):
More specifically, the system BIOS saves a system status (e.g., the contents of the register of the CPU 111 or various I/O registers) necessary for resuming the operating system or an application program which is being executed in a main memory 113 and also stores a suspend flag representing a suspend state in the backed-up CMOS memory of a real-time clock 120, and a HOT-INS flag representing that the portable computer 1 is docked in a power ON state (hot insertion) in a predetermined memory of the deskstation interface 117. The system BIOS issues a dock power OFF command to the power supply controller 123 (step C11). The dock power OFF command is a command for designating to temporarily power off the portable computer 1 for docking and set a suspend state and is sent to the portable computer 1 through the communication register of the deskstation interface 117.

Detailed Description Text (202):
The control unit 56 of the deskstation main body 5 in FIG. 13 is constituted by a microprocessor for controlling the expansion unit main body (DS) 5. In this case, a power switch ON command for designating the ON/OFF operation of the power supply, which is input by operating the control key 57, is sent to the deskstation interface 404 shown in FIG. 15, and at the same time, the power supply (PS) 59 is controlled to apply three DC power supply voltages (PV) to internal circuits. In this embodiment, when the control key 57 is operated, a power supply control line which is pulled up in advance is shorted to the ground line to output a power switch ON command for designating the ON/OFF operation of the power supply. A designation for turning on the switches S1 to S3 may be sent to the driver 66 in accordance with this control key.

Previous Doc Next Doc Go to Doc#

US005881251A

United States Patent [19]

Fung et al.

[11] Patent Number: 5,881,251

[45] Date of Patent: Mar. 9, 1999

[54] **HOT SWAP CONTROL CIRCUIT**

[75] Inventors: Laurie P. Fung, Evanston; Craig D. Lindberg, San Jose, both of Calif.

[73] Assignee: Bay Networks, Inc., Santa Clara, Calif.

[21] Appl. No.: 738,202

[22] Filed: Oct. 10, 1996

[51] Int. Cl.[6] G06F 13/00

[52] U.S. Cl. 395/283; 307/147

[58] Field of Search 395/283, 282, 395/281; 307/147, 148

[56] **References Cited**

U.S. PATENT DOCUMENTS

5,432,916	7/1995	Rahn et al.	395/283
5,473,499	12/1995	Weir	395/283
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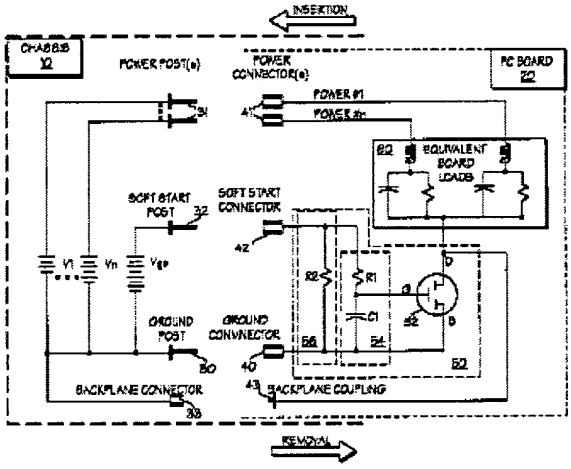
5,644,731	7/1997	Liencres et al.	395/283
5,726,505	3/1998	Wood	307/147

Primary Examiner—Glenn A. Auve
Attorney, Agent, or Firm—Blakely Sokoloff Taylor & Zafman, LLP

[57] **ABSTRACT**

A circuit board having a load is inserted into a chassis of a digital system while the system remains in operation. During insertion, a ground potential is provided to the circuit board. Next, one or more voltage potentials are provided, however, no electrical path is provided from the voltage potentials, through the load, to ground. An enhancement voltage is provided to the circuit board, allowing the load to charge. Finally, a backplane is connected to the circuit board after the load has charged. The circuit board includes a soft start circuit that allows the load to charge gracefully after the enhancement voltage is provided. In one embodiment, the soft start circuit includes an RC circuit connected to a switch which gradually turns on as the RC circuit charges, thereby providing an electrical path from the circuit board load to ground through the switch. The switch may be a MOSFET. Once the circuit board load is charged, connecting the backplane bypasses the MOSFET, thereby eliminating nearly all quiescent current flow through, and associated power dissipation in, the MOSFET. The circuit board is extracted from the chassis of the digital system by first disconnecting the backplane. When this occurs, the MOSFET is no longer bypassed by the backplane connection and quiescent current again flows through the MOSFET. Next, the enhancement voltage is removed, allowing the MOSFET to gradually turn off as the RC circuit discharges, thereby removing the electrical path from the load to ground. The voltage and ground potential are then removed.

27 Claims, 3 Drawing Sheets



US-PAT-NO: 5881251

DOCUMENT-IDENTIFIER: US 5881251 A

TITLE: Hot swap control circuit

---------- KWIC ---------

Abstract Text - ABTX (1):

A circuit board having a load is inserted into a chassis of a digital system while the system remains in operation. During insertion, a ground potential is provided to the circuit board. Next, one or more voltage potentials are provided, however, no electrical path is provided from the voltage potentials, through the load, to ground. An enhancement voltage is provided to the circuit board, allowing the load to charge. Finally, a backplane is connected to the circuit board after the load has charged. The circuit board includes a soft start circuit that allows the load to charge gracefully after the enhancement voltage is provided. In one embodiment, the soft start circuit includes an RC circuit connected to a switch which gradually turns on as the RC circuit charges, thereby providing an electrical path from the circuit board load to ground through the switch. The switch may be a MOSFET. Once the circuit board load is charged, connecting the backplane bypasses the MOSFET, thereby eliminating nearly all quiescent current flow through, and associated power dissipation in, the MOSFET. The circuit board is extracted from the chassis of the digital system by first disconnecting the backplane. When this occurs, the MOSFET is no longer bypassed by the backplane connection and quiescent current again flows through the MOSFET. Next, the enhancement voltage is removed, allowing the MOSFET to gradually turn off as the RC circuit discharges, thereby removing the electrical path from the load to ground. The voltage and ground potential are then removed.

Brief Summary Text - BSTX (10):

The circuit board includes a soft start circuit to allow the circuit board to charge gracefully after the enhancement voltage is provided. In one embodiment, the soft start circuit includes an RC circuit which charges over a predetermined time after the enhancement voltage is provided. The RC circuit is connected to a switch which gradually turns on as the RC circuit charges, thereby providing an electrical path from the circuit board load to ground

US005881251A

United States Patent [19]

Fung et al.

[11] Patent Number: 5,881,251

[45] Date of Patent: Mar. 9, 1999

[54] **HOT SWAP CONTROL CIRCUIT**

[75] Inventors: **Lawrie P. Fung**, Pleasanton; **Craig D. Lindberg**, San Jose, both of Calif.

[73] Assignee: **Bay Networks, Inc.**, Santa Clara, Calif.

[21] Appl. No.: **728,202**

[22] Filed: **Oct. 10, 1996**

[51] **Int. Cl.**[6] **G06F 13/00**

[52] **U.S. Cl.** **395/283**; 307/147

[58] **Field of Search** 395/283, 282, 395/281; 307/147, 148

[56] **References Cited**

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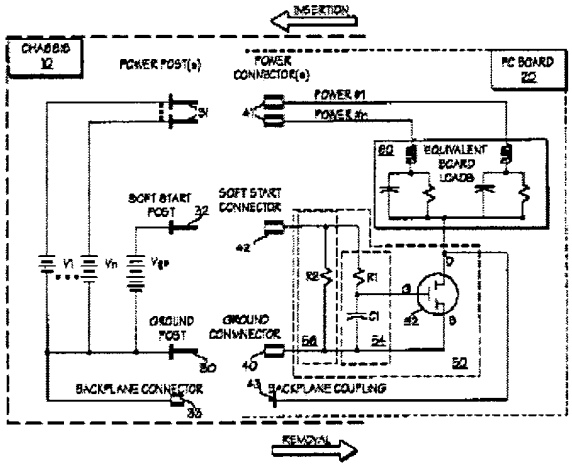
[57] **ABSTRACT**

A circuit board having a load is inserted into a chassis of a digital system while the system remains in operation. During insertion, a ground potential is provided to the circuit board. Next, one or more voltage potentials are provided, however, no electrical path is provided from the voltage potentials, through the load, to ground. An enhancement voltage is provided to the circuit board, allowing the load to charge. Finally, a backplane is connected to the circuit board after the load has charged. The circuit board includes a soft start circuit that allows the load to charge gracefully after the enhancement voltage is provided. In one embodiment, the soft start circuit includes an RC circuit connected to a switch which gradually turns on as the RC circuit charges, thereby providing an electrical path from the circuit board load to ground through the switch. The switch may be a MOSFET. Once the circuit board load is charged, connecting the backplane bypasses the MOSFET, thereby eliminating nearly all quiescent current flow through, and associated power dissipation in, the MOSFET. The circuit board is extracted from the chassis of the digital system by first disconnecting the backplane. When this occurs, the MOSFET is no longer bypassed by the backplane connection and quiescent current again flows through the MOSFET. Next, the enhancement voltage is removed, allowing the MOSFET to gradually turn off as the RC circuit discharges, thereby removing the electrical path from the load to ground. The voltage and ground potential are then removed.

27 Claims, 3 Drawing Sheets



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L3: Entry 2 of 6 File: USPT Jan 9, 2001

DOCUMENT-IDENTIFIER: US 6173352 B1
TITLE: Mobile computer mounted apparatus for controlling enablement and indicating operational status of a wireless communication device associated with the mobile computer

Detailed Description Text (5):
When the switch 210 is in a second position, the first pole 220 electrically connects the enable signal line 250 to ground 260. Connecting the enable signal line 250 to ground 260 causes the CPU 110 to disable power to the PCMCIA cards 180 and 181 via the power and interface connectors 130 and 140, respectively. Furthermore, when the switch 210 is in the second position, the second pole 230 electrically connects the power bus 200 to ground 260 thereby removing power to transmitters 190 located in the PCMCIA card 181 and embedded wireless communication device 150.

Current US Original Classification (1):
710/301

CLAIMS:

2. The apparatus recited in claim 1, wherein the circuitry for enabling the wireless communication device when the switch is in the first position and disabling the wireless communication device when the switch is in the second position electrically connects a radio frequency power bus of the wireless communication device to supply power when the switch is in the first position and electrically connects the radio frequency power bus of the wireless communication device to ground when the switch is in the second position.

4. The apparatus recited in claim 3, wherein the circuitry for enabling the wireless communication device when the switch is in the first position and disabling the wireless communication device when the switch is in the second position electrically connects an enable signal line of a central processing unit of the mobile computer to supply power when the switch is in the first position, the central processing unit connecting supply power to the PCMCIA card in response thereto, and electrically connects the enable signal line of the central processing unit of the mobile computer to ground when the switch is in the second position, the central processing unit disconnecting supply power to the PCMCIA card in response thereto.

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L2: Entry 48 of 53 File: USPT Dec 5, 1995

DOCUMENT-IDENTIFIER: US 5473499 A
TITLE: Hot pluggable motherboard bus connection method

Detailed Description Text (2):
FIG. 1 shows a basic circuit structure of the present invention. An IC card 1 connects to a motherboard 2 via a connector circuit 21 located on the motherboard 2. The ground bus of the IC card 1 is connected to the ground bus 28 of the motherboard 2 during insertion of the card into connector 21. A controller 25 controls switches 22 and 23 located between connector 21 and general purpose signal bus 26 and power bus 27, respectively, so that the switches are closed as follows. When IC card insertion detector 30 detects that an IC card 1 has been physically inserted into a connector 21 by, for example, monitoring power supply current, (see FIG. 2 step S1), the controller 25 closes the switch 23 (steps S2 to S4 as will be fully described below) to connect the motherboard power bus 27 to the IC card 1. Finally, the controller 25 closes the switch 22 (step S5) to connect the motherboard general signal bus 26 to the IC card 1.

Detailed Description Text (5):
The controller 25 also controls the switches 22 and 23 in the following manner when IC Card removal initiator 40 detects that the user wishes to physically remove an IC card 1 from the motherboard 2 (see step S6 of FIG. 3). The switches are caused to open in a certain order, specifically, the reverse order to the order in which they were closed when the IC card was first connected to the motherboard connector 21. More specifically, first the general signal bus switch 22 is opened (step S7), and then the power bus switch 23 is opened (step S8). Then, an indication is given to the user that it is alright to physically disconnect the card 1 from the motherboard connector 21 (step S9) by way of user signal 50. The ground connection is disconnected when the card is physically removed by the user.

Current US Cross Reference Classification (2):
710/302

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L2: Entry 48 of 53 File: USPT Dec 5, 1995

US-PAT-NO: 5473499
DOCUMENT-IDENTIFIER: US 5473499 A

TITLE: Hot pluggable motherboard bus connection method

DATE-ISSUED: December 5, 1995

INVENTOR-INFORMATION:

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APPL-NO: 08/ 083504 [PALM]
DATE FILED: June 30, 1993

INT-CL: [06] H02 H 9/00

US-CL-ISSUED: 361/58; 323/908, 395/750
US-CL-CURRENT: 361/58; 323/908, 710/302, 713/300

FIELD-OF-SEARCH: 361/58, 323/908, 395/750

PRIOR-ART-DISCLOSED:

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Search Selected Search ALL Clear

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☐				
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ART-UNIT: 214

PRIMARY-EXAMINER: Deboer; Todd

ATTY-AGENT-FIRM: Sughrue, Mion, Zinn, Macpeak & Seas

ABSTRACT:

A method of connecting an IC card to a motherboard involves first connecting the ground busses, then the power busses and finally the general signal busses. When the power busses are connected, a low current is allowed to flow initially, then, a predetermined period of time is allowed to elapse for equalization of IC card and motherboard voltages, then a full current is allowed to flow. A method of disconnecting an IC card from a motherboard involves first disconnecting the general signal busses, then the power busses and finally the ground busses.

2 Claims, 3 Drawing figures

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L1: Entry 1 of 2 File: USPT Mar 9, 1999

US-PAT-NO: 5881251
DOCUMENT-IDENTIFIER: US 5881251 A

TITLE: Hot swap control circuit

DATE-ISSUED: March 9, 1999

INT-CL: [06] G06 F 13/00

US-CL-ISSUED: 395/283; 307/147
US-CL-CURRENT: 710/302; 307/147

FIELD-OF-SEARCH: 395/283, 395/282, 395/281, 307/147, 307/148

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L1: Entry 2 of 2 File: USPT Dec 5, 1995

US-PAT-NO: 5473499
DOCUMENT-IDENTIFIER: US 5473499 A

TITLE: Hot pluggable motherboard bus connection method

DATE-ISSUED: December 5, 1995

INT-CL: [06] H02 H 9/00

US-CL-ISSUED: 361/58; 323/908, 395/750
US-CL-CURRENT: 361/58; 323/908, 710/302, 713/300

FIELD-OF-SEARCH: 361/58, 323/908, 395/750

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